

REMARKS

Claims 1-27 were pending in the above-referenced patent application. Claims 28-42 have been withdrawn from consideration by the Examiner. Claims 28-42 have been filed in a divisional of the above-referenced patent application, on March 22, 2005.

Claim 1 has been amended to further clarify the claimed limitations. The amendments are to place the application in better condition for allowance. Entry and consideration of the amendments are respectfully requested.

All of Claims 1-27 were rejected under 35 U.S.C. 103(a). Specifically, Claims 1, 2, 10, 11, 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,618,788 to Jacobs in view of USPN 6,748,478 Burke et al (“Burke”). Claims 3, 7, 15, 22 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs in view of USB Specification 2.0. Claims 4-6, 9, 12-14, 20 and 21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs in view of USPN 6,131,134 to Huang et al. (“Huang”). Claims 8, 16, 17 and 24-27, were rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs in view of USB Specification 2.0, and further in view of Huang.

All of the rejections are respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations. In the final office action, the claims were rejected for essentially the same reasons as the rejections in the first office action. No prima facie case of obviousness was established in the first office action or in this final office action. As such, if the claims are once again rejected, Applicants respectfully request that the final rejection be withdrawn.

Jacobs is directed to remotely controlling an ATA device via a packet-based interface, where a remote host constructs command blocks corresponding to the ATA register-delivered commands that it would like executed. These command blocks are packetized and transported to a packet-to-ATA format bridge. At the bridge, each command block is parsed, and appropriate ATA read or write register commands are performed. The bridge performs requested data transfers via the packet-based interface. This allows a non-ATAPI ATA device to connect externally to a host computer, e.g., via a USB plug-and-play packet interface (Abstract).

Jacobs' teaching are therefore directed to connecting an ATA device to a host using a packet-based interface. Fig. 5 of Jacobs shows the packet-based interface implemented in the bridging circuit 156, to connect the logical ATA device 140 to the host 130. Importantly, Jacobs states that the logical ATA device 140 can include two physical ATA devices (DEV0 and DEV1) on the same ATA bus in the ATA device 140. As such, Jacobs is explicit in its teachings that to connect two physical ATA devices to a host, the two physical ATA devices are connected to the same ATA bus in the logical ATA device 140. The logical ATA device 140 is in turn connected to the host 130 via one bridging circuit 156. Therefore, according to Jacobs' explicit teachings, connecting two ATA devices to the host 130 is not done by employing two bridging circuits 156, with one bridging circuit 156 per ATA device, rather in Jacobs a single bridging circuit 156 is used to connect two ATA devices that are on an ATA bus to the host 130.

As such, unlike the claimed invention herein, Jacobs does not disclose multiple bridges connected to a USB controller. Jacobs only mentions two ATA devices on an ATA bus connected to one bridge 156, and the one bridge 156 is connected to the host 130. Further, as the Examiner also admits, Jacobs does not disclose multiple bridges 156 connected to a USB controller, wherein an ATA device is connected to each bridge 156. However, the Examiner states that Jacobs can be modified to achieve the claimed invention, because connecting multiple devices to a USB controller via multiple bridges is known in the prior art. The Examiner provides Burke as an

example of multiple bridges, and then states that the motivation for modifying Jacobs is to connect multiple ATA devices to the host 130.

Applicants respectfully traverse the Examiner's contentions. Indeed, despite the Examiner's above-suggested motivation, Jacobs itself (Fig. 5) teaches away from the claimed invention by providing a mechanism whereby when two ATA devices are to be connected to the host 130, the two ATA devices are connected to one ATA bus which in device 140 is then connected to one bridge 156 that is coupled to the host 130. There is no teaching or suggestion in Jacobs about connecting two bridges 156 to the host 130. Indeed, the communications stacks in Figs. 7 and 8 provide no teachings or suggestions as such, and are for using one bridge 156. Using multiple bridges 156 is also incompatible with the communication stacks in Figs. 7 and 8 of Jacobs. If the Examiner believes otherwise, Applicants respectfully request the Examiner specifically point to disclosure in Jacobs where multiple bridges are supported by the communication stacks in Figs. 7 and 8.

As per Claim 1 herein, despite the Examiner's interpretation, Jacobs (col. 5, lines 29-33, relied on by the Examiner) does not disclose a USB system for data communication between a processor and IDE devices, comprising a plurality of IDE devices, and a plurality of USB-to-IDE bridges, wherein each IDE device is connected to a respective USB-to-IDE bridge, as required by Claim 1. Instead, in col. 5, lines 29-33, Jacobs simply states: "And although the following discussion will focus on a single ATA DEV0, ATA device 140 could also incorporate two physical devices, one functioning as DEV0 and the other as DEV1 on the same ATA bus." Jacobs mentions that the ATA device 140 (Fig. 5) can incorporate two devices functioning on the same ATA bus in the device 140. One of the devices in the device 140 functions as DEV0 and the other as DEV1 on the same ATA bus in device 140. Jacobs does not disclose a plurality of IDE devices, each coupled to a IDE-to-USB bridge that is connected to a USB controller, as required by Claim 1 (i.e., Jacob's devices DEV0 and DEV1 function on an ATA bus in the device 140 that is connected

to the cabling bridge 156). Indeed, Even when Jacobs utilizes two devices DEV0 and DEV1 in the ATA device 140, *Jacobs still uses only one USB-to-ATA bridging cable 156 for the two devices DEV0 and DEV1*, not a plurality of USB-to-IDE bridges corresponding to a plurality of IDE devices, as required by Claim 1.

In addition, as Jacobs clearly specifies, the element 130 is a host machine, and not a USB controller as required by Claim 1. The only mention of a USB controller in Jacobs (relied on by the Examiner) is in the prior art listed by Jacobs, but nowhere does Jacobs mention a USB controller in the host 130. In all of the detailed diagrams of the invention of Jacobs, there is mention of a USB controller being used in the host 130. Further, Jacobs does not disclose a USB controller, wherein the USB-to-IDE bridges are connected to the USB controller, whereby the processor can communicate with the IDE devices via the USB controller. Nor does Jacobs mention a USB controller that can be connected to multiple USB-to-IDE bridges for communication therewith.

Further, it is respectfully suggested that despite the Examiner's taking Official Notice, there is no teaching in the prior art of connecting multiple IDE devices to multiple USB-to-IDE bridges that are connected to a USB controller. Burke is directed to a system and method of configuring processing resources for communication with one or more devices coupled to a data bus through a bridge. Resources at a processing system are configured to communicate with the bridge as a transparent bridge or a non-transparent bridge depending on how the processing system may be implemented in a processing platform (Abstract). Burke (Fig. 1, relied on by the Examiner), shows multiple bridges (BRIDGE 1... 4), but each of these bridges is connected to a HOST BRIDGE, rather than to a USB controller as claimed. There is no mention of USB or a USB controller anywhere in Burke. According to Burke (col. 3, lines 12-16) the HOST BRIDGE is a bridge for coupling a host bus to a second bus to facilitate communication between a processing system and devices coupled to the second bus.

Referring to col. 3, lines 33-49, Burkes describes Fig. 1 as showing a CPU 2 is coupled to a main memory 4 for executing processes. The CPU 2 is coupled through a host bridge 6 to a bus configuration 14. The bus configuration 14 comprises a plurality of data busses 10 coupled by bridges 8. One or more peripheral devices 12 may be coupled to a bus 10 for communication with other peripheral devices 12 and/or processes executing on the CPU 2. The CPU 2 and main memory 4 may host device drivers to enable communication between application processes and the peripheral devices 12 according to a communication protocol. However, embodiments of the present invention are limited in this respect and the peripheral devices 12 may communicate with application processes using other techniques.

As such, Burke does not disclose multiple bridges according to the claimed invention herein. Burke does not disclose multiple IDE devices that are connected one-to-one to multiple USB-to-IDE bridges, wherein the multiple bridges are connected to a USB controller, as claimed herein (Claim 1).

For at least these reasons, rejection of Claim 1, and all claims dependent therefrom should be withdrawn.

Claims 10 and 18 were rejected for substantially the same reasons as rejection of Claim 1. As such, for at least the reasons provided above in relation to Claim 1, it is respectfully submitted that rejection of Claims 10, 18, and all claims dependent therefrom, should be withdrawn.

As per Claim 4, as the Examiner also states, Jacobs does not disclose a system wherein a IDE device can be utilized in hot plugging. The Examiner states that Huang discloses such a feature, and that it would have been obvious to modify Jacobs according to Huang to achieve the claimed invention. However, Huang is directed to USB converter working between an old

interface (legacy interface) and a USB interface, to enable the hot PnP function on the system (col. 3, lines 1-3; col. 5, lines 30-33). Huang's USB converter inputs legacy interface (non USB) signals and outputs USB signals. The USB converter of Huang is incompatible with Jacobs' smart cable 150 (Jacobs, Fig. 5). In Fig. 5 of Jacobs, Huang's USB converter cannot be connected between the smart cable 150 and the USB port 132. The USB plug 154 of Jacobs' cable 150 is already in USB format, not legacy format as Huang requires, and as such it is incompatible with input to Huang's USB converter. Nor can Huang's USB converter be connected between the ATA device 140 and the ATA connector 152 because Huang's USB connector outputs USB signals but the connector 152 expects ATA signals.

A combination of Jacobs and Huang is non-functional. It is respectfully submitted that this non-functionality is a clear indication that combining Jacobs and Huang not only does not teach the claimed invention, but to make it functional for any purpose, requires substantial changes non-obvious changes to the Jacobs and/or Huang. This goes against the obviousness rejection by the Examiner. Further, neither of the references provides a motivation for a combination thereof. For at least these reasons, rejection of Claim 4 should be withdrawn.

As per Claims 7, 15, 22, neither Jacobs nor Huang provide any motivation for utilizing a USB hub, and neither disclose that such a feature would even work with their system. Again, their combination is non-functional, which goes against the Examiner's obviousness rejection. Therefore, it is respectfully requested that rejection of Claims 7, 15, 22, and all claims dependent therefrom, should be withdrawn.

Rejection of Claims 5, 6 and 9 is respectfully traversed for at least the reasons provided in relation to Claim 5. Further, as per Claim 6, Jacobs (col. 1, lines 49-51), only allows up to two ATA devices (e.g., devices 44 and 46 on FIG. 1) to share the ATA bus 42. As such, only up to two devices can be incorporated in the device 140, connected to one cable 150.

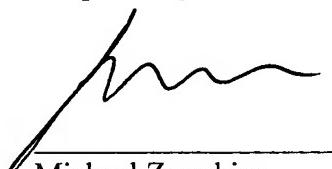
Claims 12, 13, 14, 20 and 21 were rejected for substantially the same reasons as rejection of Claims 5, 6 and 9, and should therefore be allowed for at least the reasons provided in relation to Claims 1, 5, 6 and 9. Further, rejection of Claims 8, 16, 17, 24-27 should be withdrawn for at least the reasons provided in relation to Claims 1, 5-7, 9, 15 and 22.

CONCLUSION

For the foregoing, and other, reasons Applicants believe that the rejected claims should be allowed. Reconsideration and allowance of the rejected claims are respectfully requested.

Please continue to direct all communications regarding the above-referenced patent application to the principal agent of record.

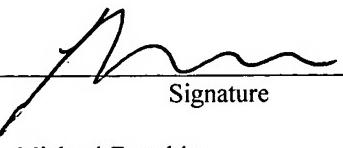
Respectfully Submitted,



Michael Zarrabian
Reg. No. 39,886

CERTIFICATE OF MAILING

I hereby certify that this correspondence or paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on March 22, 2005.

By _____

Signature
Michael Zarrabian
Typed Name of Person Mailing Paper or Fee